PATENT ABSTRACTS OF JAPAN

(11)Publication number:

61-013667

(43) Date of publication of application: 21.01.1986

₹51)Int.CI.

H01L 29/78

H01L 29/08 H01L 29/52

(21)Application number: 59-131975

(71)Applicant: TOSHIBA CORP

(22)Date of filing:

28.06.1984

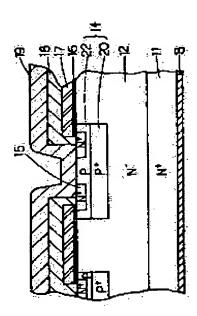
(72)Inventor: SUZUKI KAZUAKI

(54) INSULATED GATE TYPE FIELD-EFFECT TRANSISTOR

(57)Abstract:

PURPOSE: To increase breakdown resistance by using a semiconductor substrate in which a P+ layer in high impurity concentration is buried previously to the lower section of a P type base region in a channel section in the N type semiconductor substrate.

CONSTITUTION: An N- type epitaxial layer 12 is formed onto one surface of an N+ type high-concentration Si substrate 11, and a drain region is shaped by these substrate 11 and layer 12. A channel-section base region 14 consisting of a P+ base layer 20 and a P base layer 22 is formed into the layer 12 while N+ type source regions 15 are each shaped into the layer 22. The region 14 forms a base in a parastic transistor. Gate electrodes 17 are formed on the region 12 through gate insulating films 16 extended up to the upper sections of the region 14 and the regions 15. A lower section in the region 14 is formed in the P+ layer in high concentration in a double diffused type MOSFET having said constitution, thus preventing the breakdown of an FET generated by



the operation of a parastic N-P-N transistor on the reverse recovery of a free wheel diode.

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

Date of requesting appeal against examiner's

decision of rejection]
[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office